## State Machine Design

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This presentation will

- Define a state machine.
- Provide several examples of everyday items that are controlled by state machines.
- Illustrate the block diagram for a state machine.
- Review the design steps in the state machine design process.
- Provide an example of a simple state machine design.


## Definition of a State Machine

## State Machine

A synchronous sequential circuit, consisting of a sequential logic section and a combinational logic section, whose outputs and internal flip-flops progress through a predictable sequence of states in response to a clock and other input signals.*

## Examples of State Machines

Many everyday devices are controlled by state machines.


Vending Machine

## State Machine Block Diagram



## State Machine Design Steps

1. Create State Graph
2. Determine State Variables and Assign
3. Encode Outputs to States
4. Create State Transition Table
5. Write and Simplify Design Equations
6. Design Circuit

## Anatomy of a State Graph



## State Machine Design Example

Example:
Design a state machine that will count out the last four digits of the phone number 585-476-4691.


In addition to the clock input, this design has a second input called Enable (EN). Whenever the Enable is a logic (1), the outputs will continuously cycle through the four values 4,6,9,1. Whenever the Enable is a logic (0), the outputs will hold at their current values.

For this design any form of combinational logic may be used, but the sequential logic must be limited to $D$ flip-flops.


## Step \#1: Create State Graph



## Step \#2: Determine State Variables and Assign



## Step \#3: Encode Outputs to States



## Step \#3: Create State Transition Table

| $\begin{aligned} & \stackrel{0}{0} \\ & \stackrel{\rightharpoonup}{\mathbb{D}} \end{aligned}$ | Inputs |  |  | $\begin{aligned} & \stackrel{(N)}{\stackrel{\rightharpoonup}{0}} \\ & \stackrel{\rightharpoonup}{\tilde{D}} \end{aligned}$ | Outputs |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Present State |  | $\begin{array}{\|l\|} \hline \text { Input } \\ \hline \text { EN } \\ \hline \end{array}$ |  | Next State |  | F/FInputs |  | Encoded Outputs |  |  |  |
|  | Qa | Qb |  |  | Qa* | Qb* | Da | Db | C3 | C2 | C1 | C0 |
| So | 0 | 0 | 0 | S0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| so | 0 | 0 | 1 | S1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| S1 | 0 | 1 | 0 | S1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| S1 | 0 | 1 | 1 | S2 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| S2 | 1 | 0 | 0 | S2 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| S2 | 1 | 0 | 1 | S3 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| S3 | 1 | 1 | 0 | S3 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| S3 | 1 | 1 | 1 | S0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## Step \#4: Write and Simplify Design Equations

$\mathrm{Da}=\overline{\mathrm{Qa}} \mathrm{QbEN}+\mathrm{Qa} \overline{\mathrm{Qb}} \overline{\mathrm{EN}}+\mathrm{Qa} \overline{\mathrm{Qb}} \mathrm{EN}+\mathrm{Qa} \mathrm{Qb} \overline{\mathrm{EN}}$
$\mathrm{Da}=\overline{\mathrm{Qa}} \mathrm{Qb} \mathrm{EN}+\mathrm{QaEN}+\mathrm{Qa} \overline{\mathrm{Qb}}$
$\mathrm{Db}=\overline{\mathrm{Qa}} \overline{\mathrm{Qb}} \mathrm{EN}+\overline{\mathrm{Qa}} \mathrm{Qb} \overline{\mathrm{EN}}+\mathrm{Qa} \overline{\mathrm{Qb}} \mathrm{EN}+\mathrm{Qa} \mathrm{Qb} \overline{\mathrm{EN}}$
$\mathrm{Db}=\mathrm{Qb} \overline{\mathrm{EN}}+\overline{\mathrm{Qb}} \mathrm{EN}$
$\mathrm{Db}=\mathrm{Qb} \oplus \mathrm{EN}$
$\mathrm{C} 3=\mathrm{Qa} \overline{\mathrm{Qb}} \overline{\mathrm{EN}}+\mathrm{Qa} \overline{\mathrm{Qb}} \mathrm{EN}=\overline{\mathrm{Qa} \overline{\mathrm{Qb}}}$
$\mathrm{C} 2=\overline{\mathrm{Qa}} \overline{\mathrm{Qb}} \overline{\mathrm{EN}}+\overline{\mathrm{Qa}} \overline{\mathrm{Qb}} \mathrm{EN}+\overline{\mathrm{Qa}} \mathrm{Qb} \overline{\mathrm{EN}}+\overline{\mathrm{Qa}} \mathrm{QbEN}=\overline{\mathrm{Qa}}$
$\mathrm{C} 1=\overline{\mathrm{Qa}} \mathrm{Qb} \overline{\mathrm{EN}}+\overline{\mathrm{Qa}} \mathrm{Qb} \mathrm{EN}=\overline{\mathrm{Qa}} \mathrm{Qb}$
$\mathrm{CO}=\mathrm{Qa} \overline{\mathrm{Qb}} \overline{\mathrm{EN}}+\mathrm{Qa} \overline{\mathrm{Qb}} \mathrm{EN}+\mathrm{Qa} \mathrm{Qb} \overline{\mathrm{EN}}+\mathrm{Qa} \mathrm{Qb} \mathrm{EN}=\mathrm{Qa}$

## Step \#5: Circuit Design



## Block Diagram / Schematic



