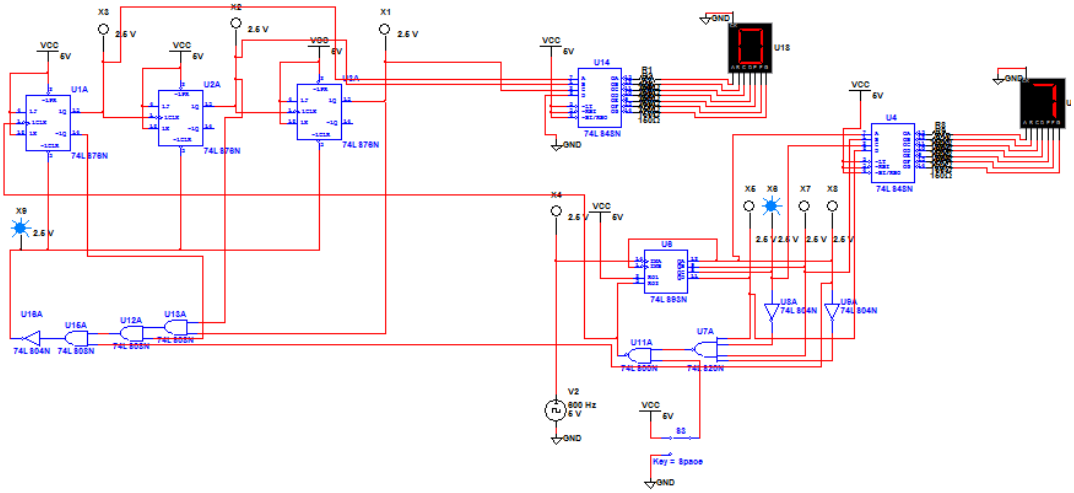
Grant Sample, 1B

Sixty Second Counter Report Format

- Problem: Design a digital Sixty Second Timer that counts from 00 to 60.

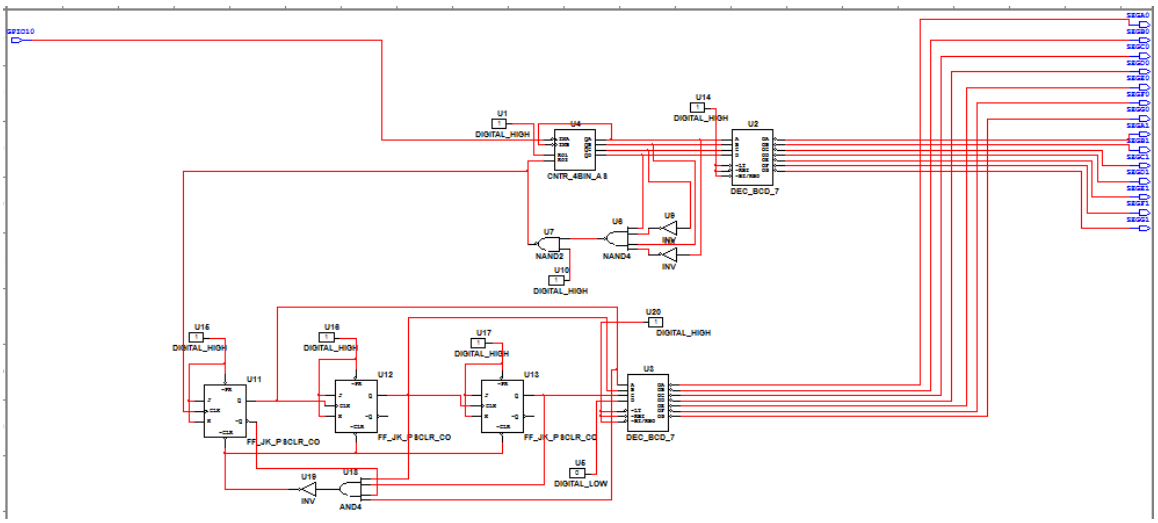
- Materials Used:
  - 74ls76
  - 74ls93
  - 74ls48
  - Seven Segment Display, Common Cathode
  - 150Ω Resistors
  - Various AOI Logic Components

- Simulation:



Using the components listed above, this is the simulation design I created to create a 60 second counter. There are two different types of counters used in this design. Three 74ls76's were used to create the counter that ranged from 0 to 6. This represented the 10s place. The clock for this is driven from the reset of the second counter circuit. This counter is used for the 1s place and utilizes a 74ls93. The outputs of both counter circuits are wired to a Seven Segment Driver chip (74ls48) which translates the binary code into lighting sequences for the seven segment displays. All of this is wired to AOI logic which forces the circuit to reset after it counts to 60, starting it back at 0.

- DLB:



Using the same basic circuit design, I implemented the 60 Second Counter into DLB configuration and uploaded it to the DLB board. The clock input for the circuit was GPIO10, which had the clock wired into it. This circuit is the same as the previous design, except for minor changes that allowed it to be uploaded to the DLB, elimination the need for the laborious task of bread boarding the circuit. After upload, the circuit immediately goes into effect, starting at 00, and counting up at a speed based on the clock input, until it reaches 60. Then, the AOI tells it at 61 to reset back to 00, creating a 00-60 second counter.