Summary

Boolean & DeMorgan's Theorems

1) $X \cdot 0 = 0$

2) $X \cdot 1 = X$

3) $X \cdot X = X$

4) $X \cdot \overline{X} = 0$

5) $X + 0 = X$

6) $X + 1 = 1$

7) $X + X = X$

8) $X + \overline{X} = 1$

9) $\overline{\overline{X}} = X$

10A) $X \cdot Y = Y \cdot X$

10B) $X + Y = Y + X$

Commutative Law

11A) $X(YZ) = (XY)Z$

11B) $X + (Y + Z) = (X + Y) + Z$

Associative Law

12A) $X(Y + Z) = XY + XZ$

12B) $(X + Y)(W + Z) = XW + XZ + YW + YZ$

Distributive Law

13A) $X + \overline{X}Y = X + Y$

13B) $\overline{X} + XY = \overline{X} + Y$

13C) $X + \overline{X}\,\overline{Y} = X + \overline{Y}$

13D) $\overline{X} + X\overline{Y} = \overline{X} + \overline{Y}$

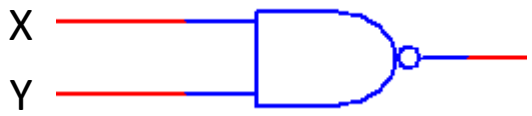
Consensus Theorem

14A) $\overline{X\,Y} = \overline{X} + \overline{Y}$

14B) $\overline{X + Y} = \overline{X}\ \ \overline{Y}$

DeMorgan's

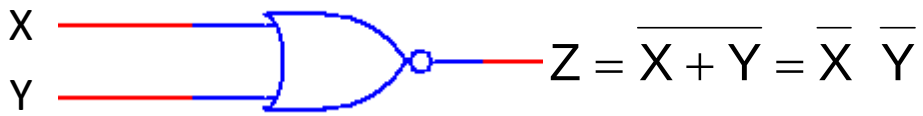
NAND Gate



$$Z = \overline{X\,Y} = \overline{X} + \overline{Y}$$

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate



X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate – Exclusive OR

$$Z = \overline{X}\,Y + X\,\overline{Y} = X \oplus Y$$

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

XNOR Gate – Exclusive NOR

$$Z = \overline{X}\,\overline{Y} + X\,Y = \overline{X \oplus Y}$$

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

Logic Design with XOR & XNOR

Example

Algebraically manipulate the logic expression for F_1 so that XOR and XNOR gates can be used to implement the function. Other AOI gates can be used as needed.

$$F_1 = X\,\overline{Y}\,Z + \overline{X}\,Y\,Z + \overline{X}\,\overline{Y}\,\overline{Z} + X\,\overline{Y}\,Z$$

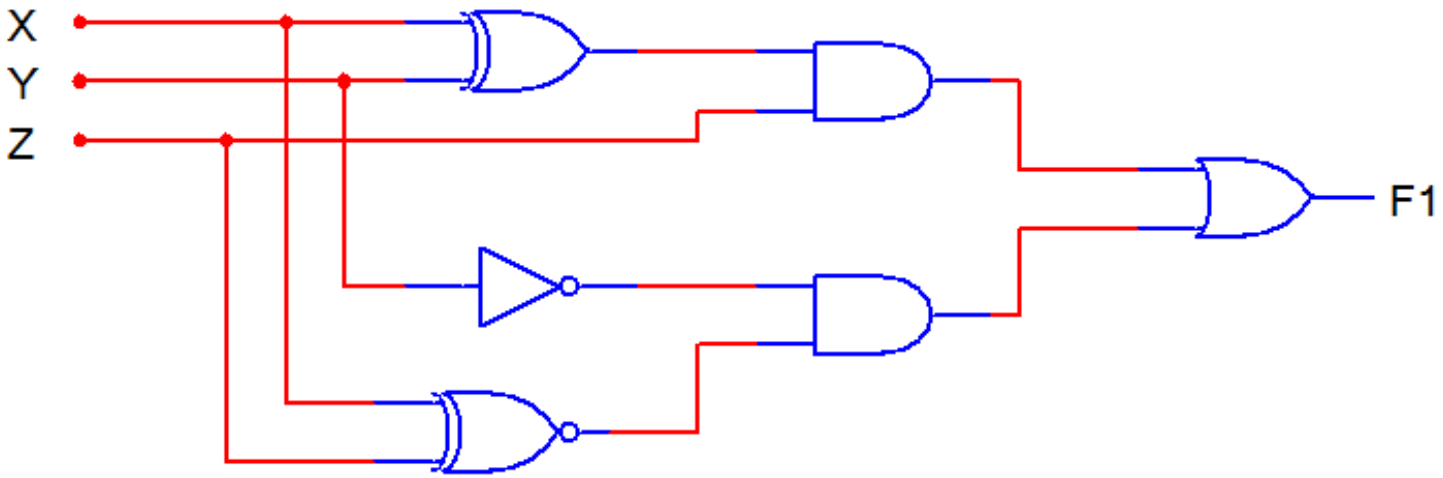
Logic Design with XOR & XNOR

Solution

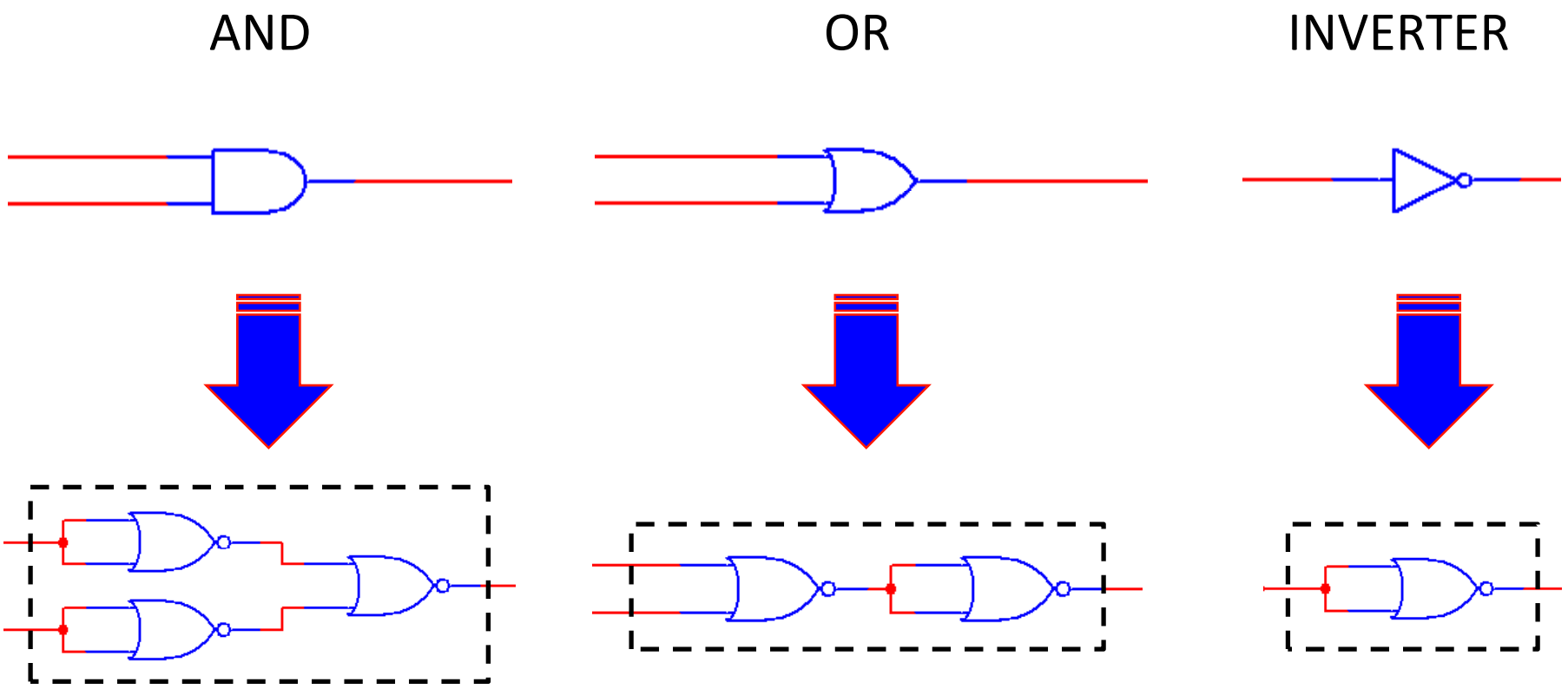
$$F_1 = X\,\overline{Y}\,Z + \overline{X}\,Y\,Z + \overline{X}\,\overline{Y}\,\overline{Z} + X\,\overline{Y}\,Z$$

$$F_1 = Z\left(X\,\overline{Y} + \overline{X}\,Y\right) + \overline{Y}\left(\overline{X}\,\overline{Z} + X\,Z\right)$$

$$F_1 = Z\left(X \oplus Y\right) + \overline{Y}\left(\overline{X \oplus Z}\right)$$

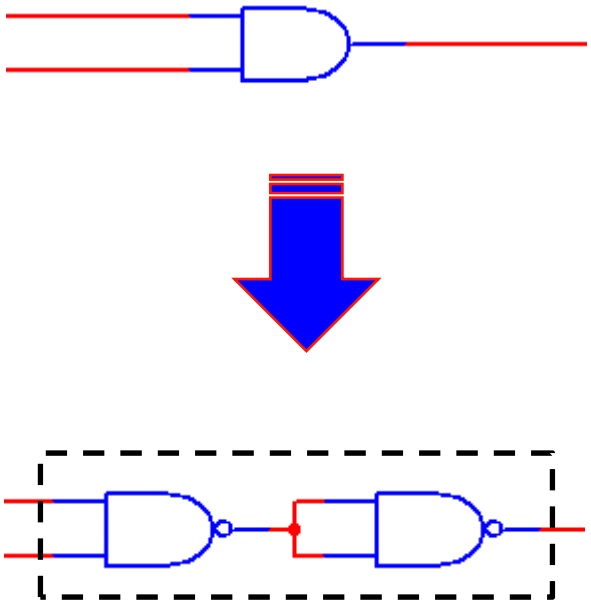


NOR Gate Equivalent of AOI Gates

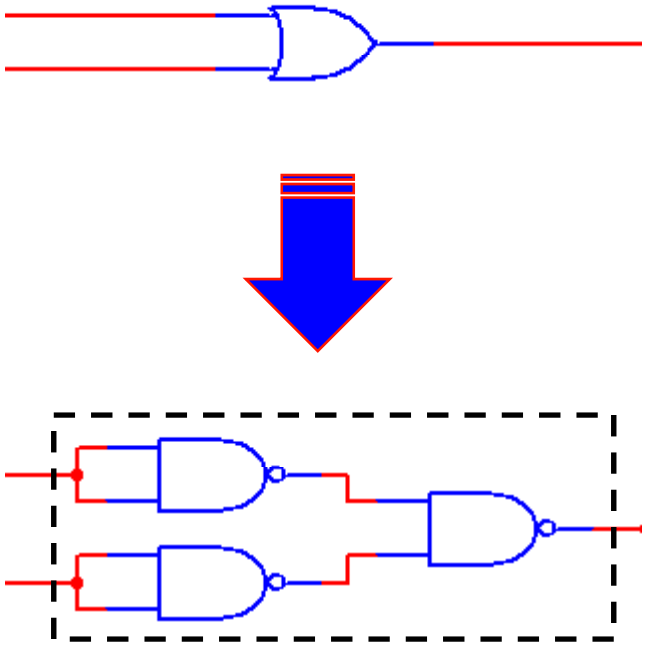


NAND Gate Equivalent to AOI Gates

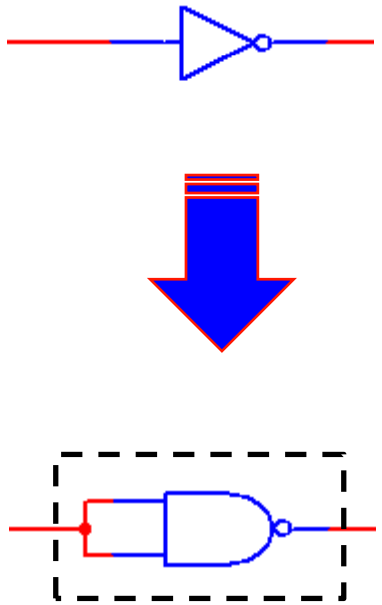
AND



OR



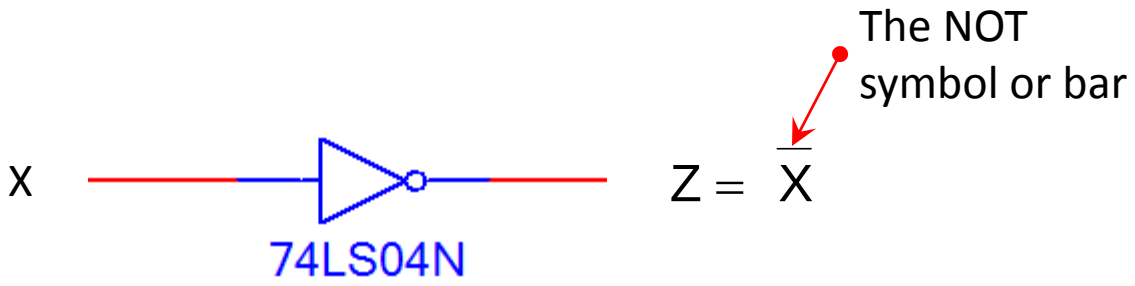
INVERTER



Common Electronic Symbol & Units

Quantity	Symbol	Unit
Current	I	Ampere (A)
Voltage	V	Volt (V)
Resistance	R	Ohm (Ω)
Frequency	f	Hertz (Hz)
Capacitor	C	Farad (F)
Inductance	L	Henry (H)
Power	P	Watt (W)

The INVERTER Gate



X	Z
0	1
0	1
1	0
1	0

Z is TRUE whenever X is NOT TRUE

The inverter is sometimes called the NOT gate.

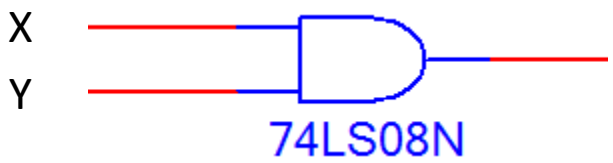
The OR Gate

$Z = X + Y$

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

Z is TRUE whenever X OR Y are TRUE

The AND Gate



$$Z = X \times Y = X \bullet Y = XY$$

Three ways to write the AND symbol

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Z is TRUE whenever X AND Y are TRUE

Parts of a Digital Signal

Amplitude:
For digital signals, this will ALWAYS be 5 volts.

Period:
The time it takes for a periodic signal to repeat. (seconds)

Frequency:
A measure of the number of occurrences of the signal second. (Hertz, Hz)

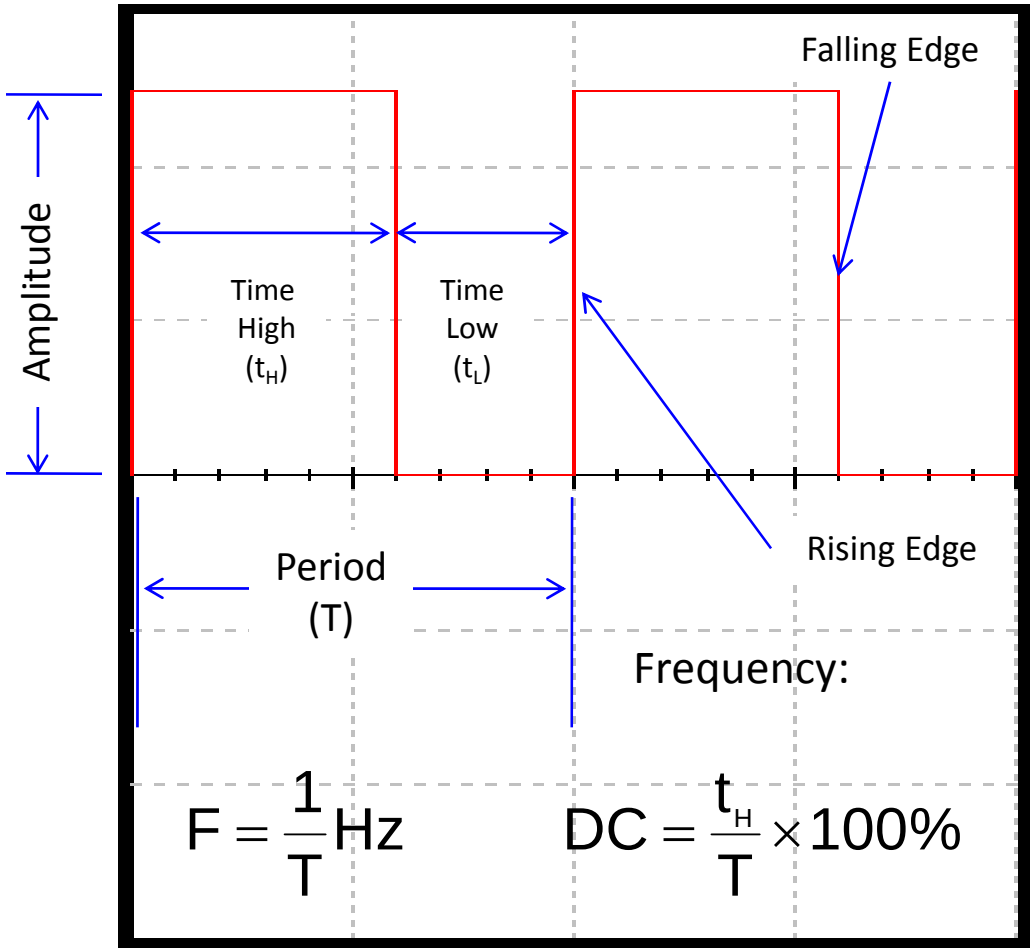
Time High (t_H):
The time the signal is at 5 v.

Time Low (t_L):
The time the signal is at 0 v.

Duty Cycle:
The ratio of t_H to the total period (T).

Rising Edge:
A 0-to-1 transition of the signal.

Falling Edge:
A 1-to-0 transition of the signal.



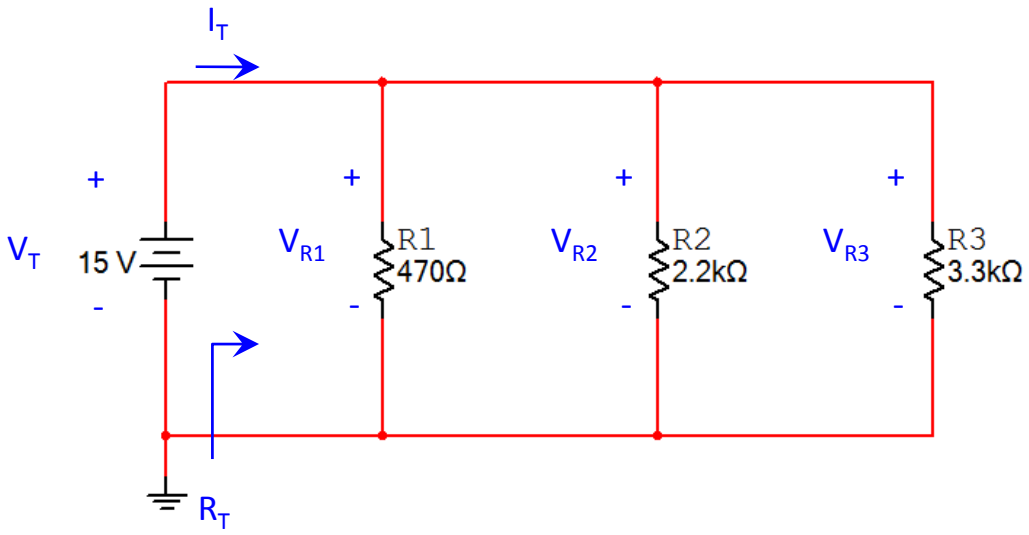
Parallel Circuits

Characteristics of a Parallel Circuit

- The voltage across every parallel component is equal.
- The total resistance (R_T) is equal to the reciprocal of the sum of the reciprocal:

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \qquad R_T = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

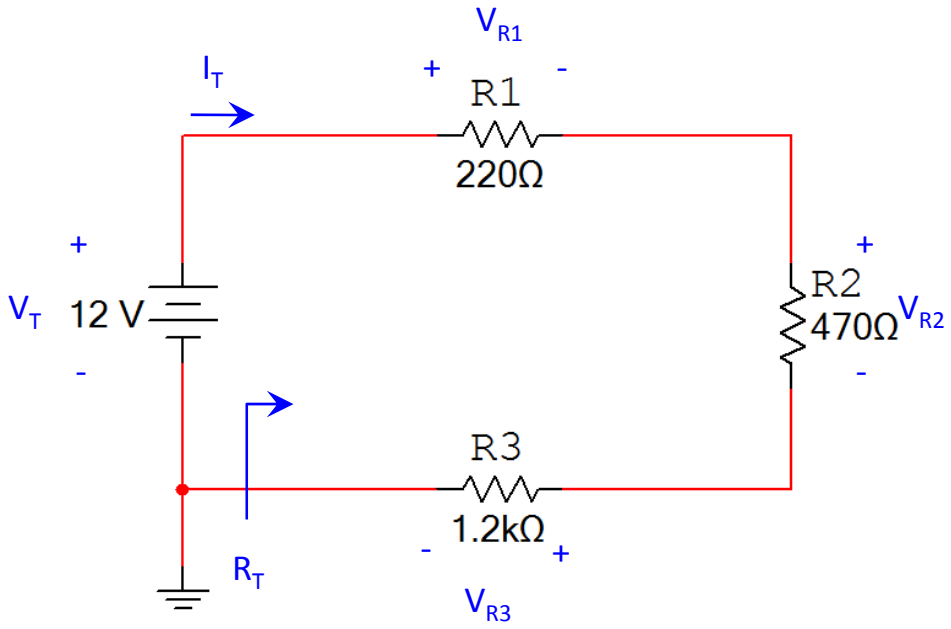
- The sum of all of the currents in each branch ($I_{R1} + I_{R2} + I_{R3}$) is equal to the total current (I_T). This is called *Kirchhoff's* Current Law.



Series Circuits

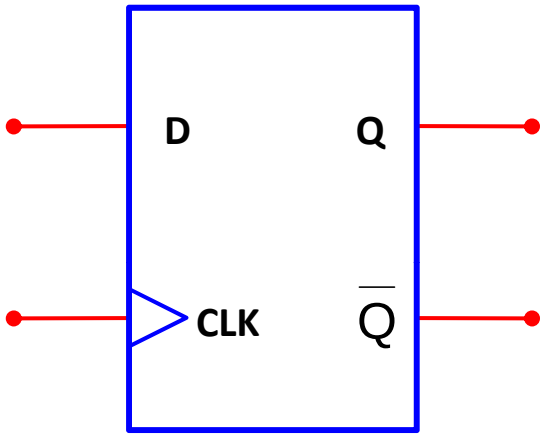
Characteristics of a series circuit

- The current flowing through every series component is equal.
- The total resistance (R_T) is equal to the sum of all of the resistances (i.e., $R_1 + R_2 + R_3$).
- The sum of all of the voltage drops ($V_{R1} + V_{R2} + V_{R2}$) is equal to the total applied voltage (V_T). This is called *Kirchhoff's* Voltage Law.



POS & NEG Edge Triggered D

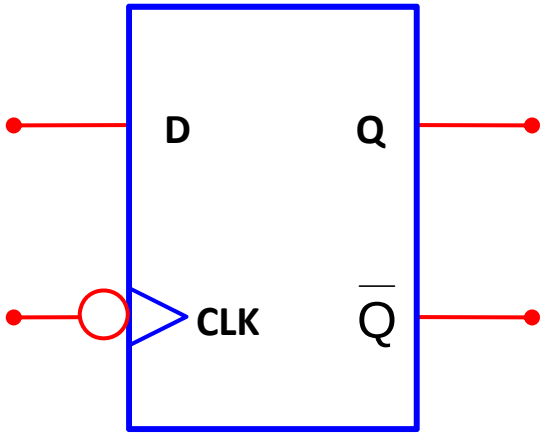
Positive Edge Trigger



D	CLK	Q	$\overline{Q}$
0	↑	0	1
1	↑	1	0

↑ : Rising Edge of Clock

Negative Edge Trigger

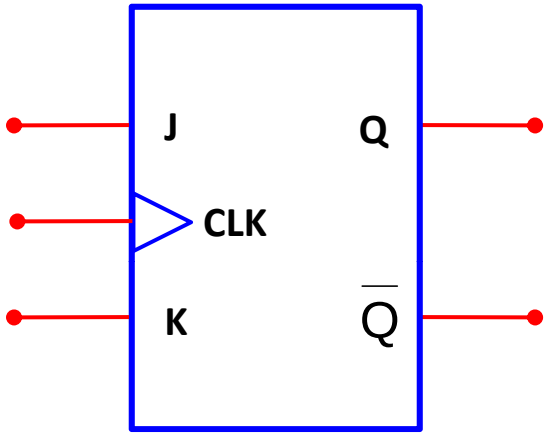


D	CLK	Q	$\overline{Q}$
0	↓	0	1
1	↓	1	0

↓ : Falling Edge of Clock

POS & NEG Edge Triggered J/K

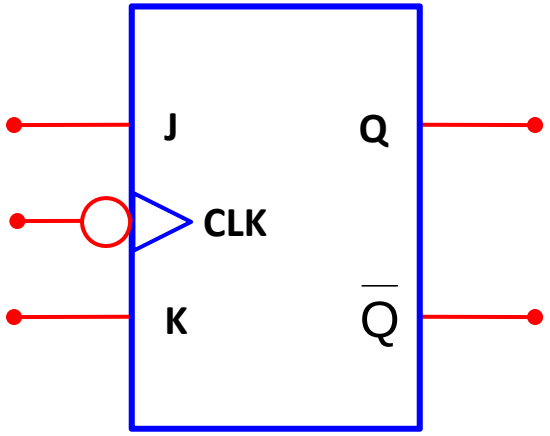
Positive Edge Trigger



J	K	CLK	Q
0	0	↑	Q_0
0	1	↑	0
1	0	↑	1
1	1	↑	$\overline{Q}_0$

↑ : Rising Edge of Clock

Negative Edge Trigger



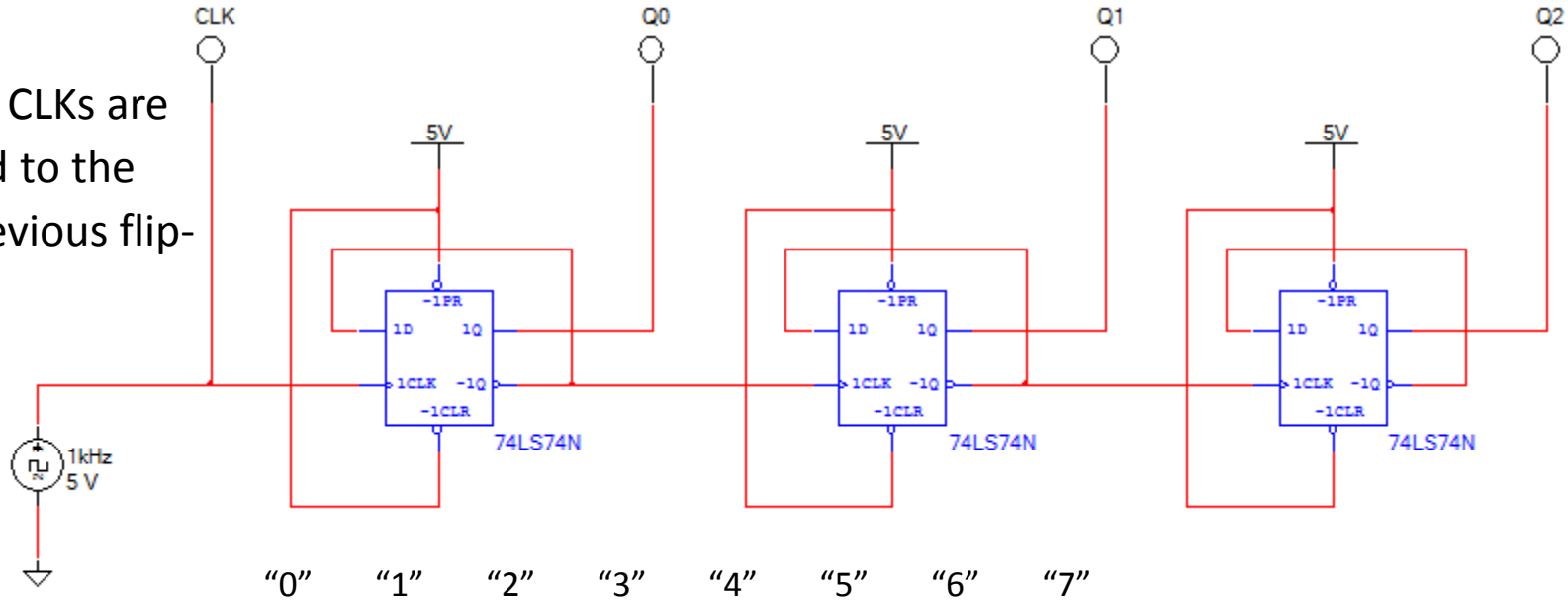
J	K	CLK	Q
0	0	↓	Q_0
0	1	↓	0
1	0	↓	1
1	1	↓	$\overline{Q}_0$

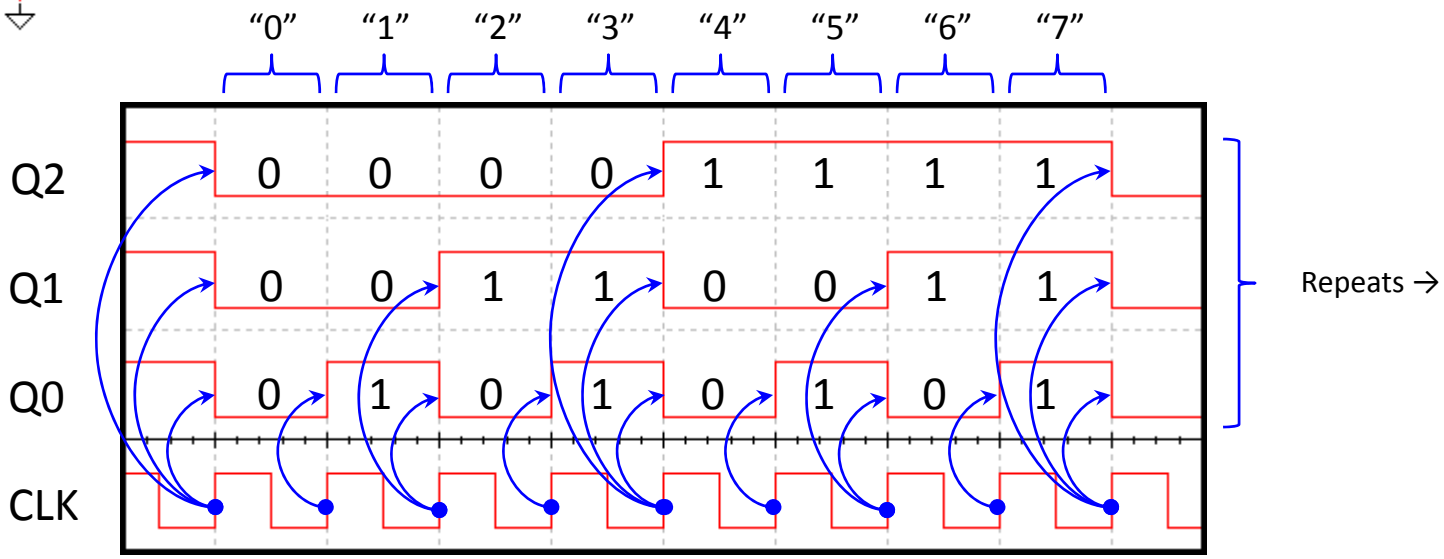
↓ : Rising Edge of Clock

Asynchronous Counter

Up Counter – D-Flip Flops – 3 Bit

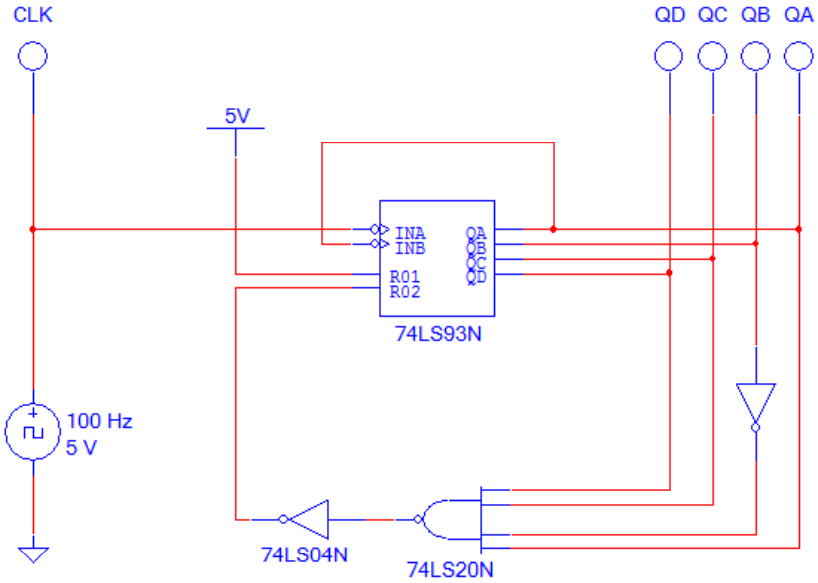
Note: The CLKs are connected to the $\overline{Q}$ of the previous flip-flop.

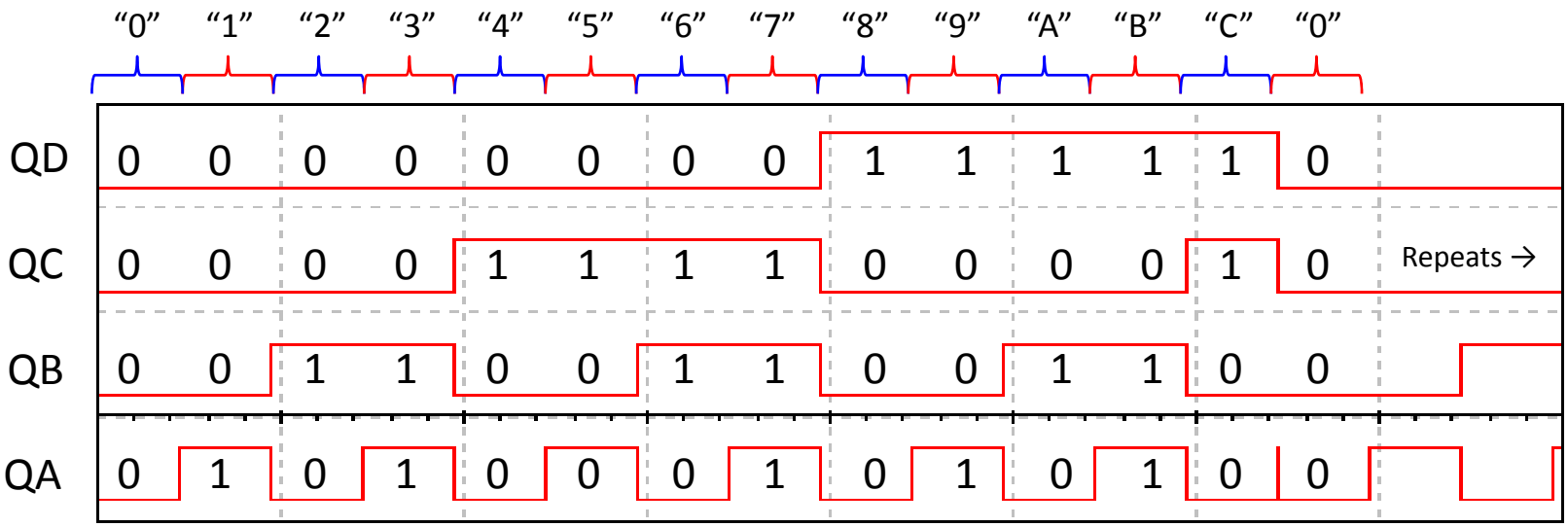




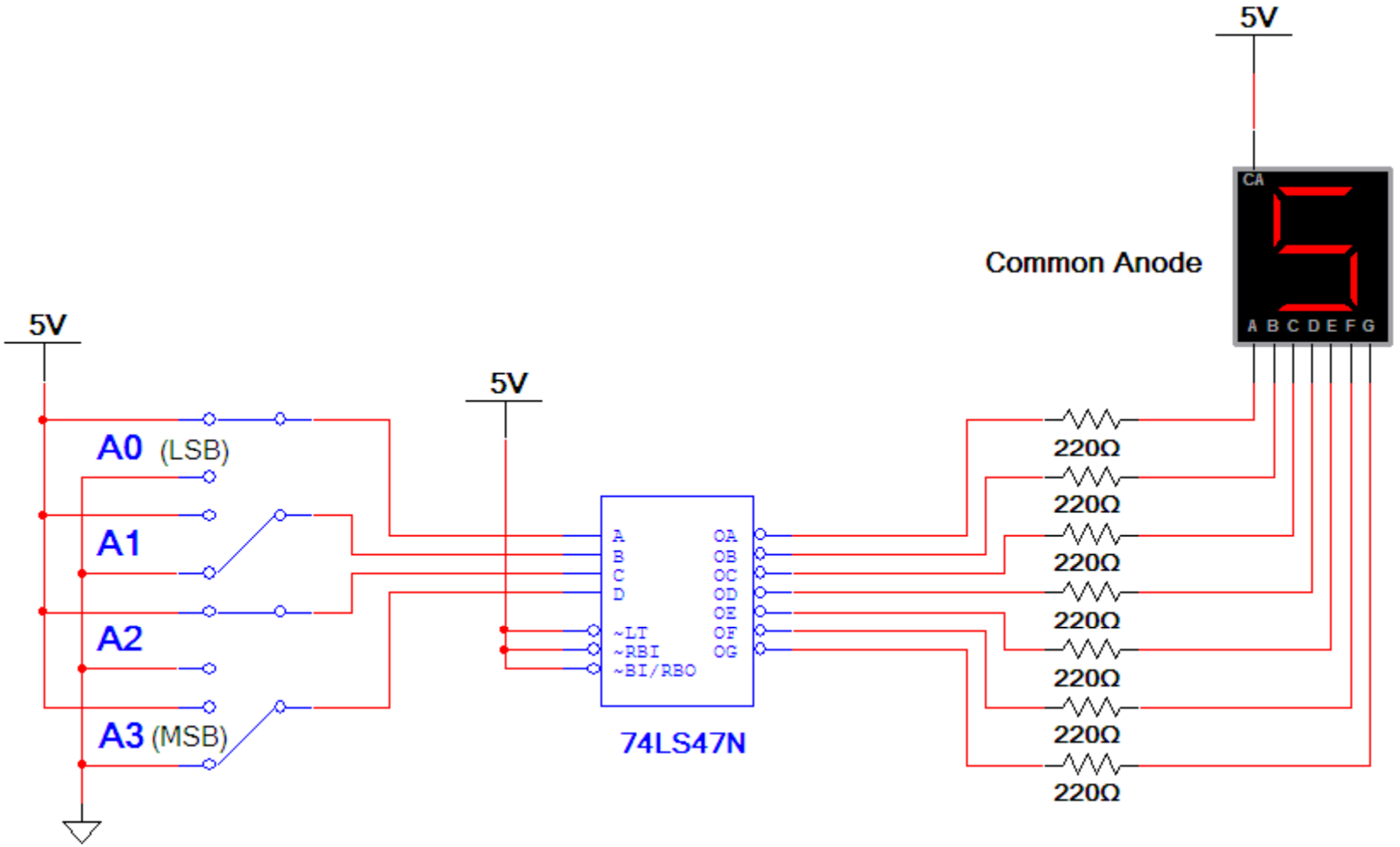
Design Example: Timing

4-Bit Asynchronous
Modulus-13 Counter

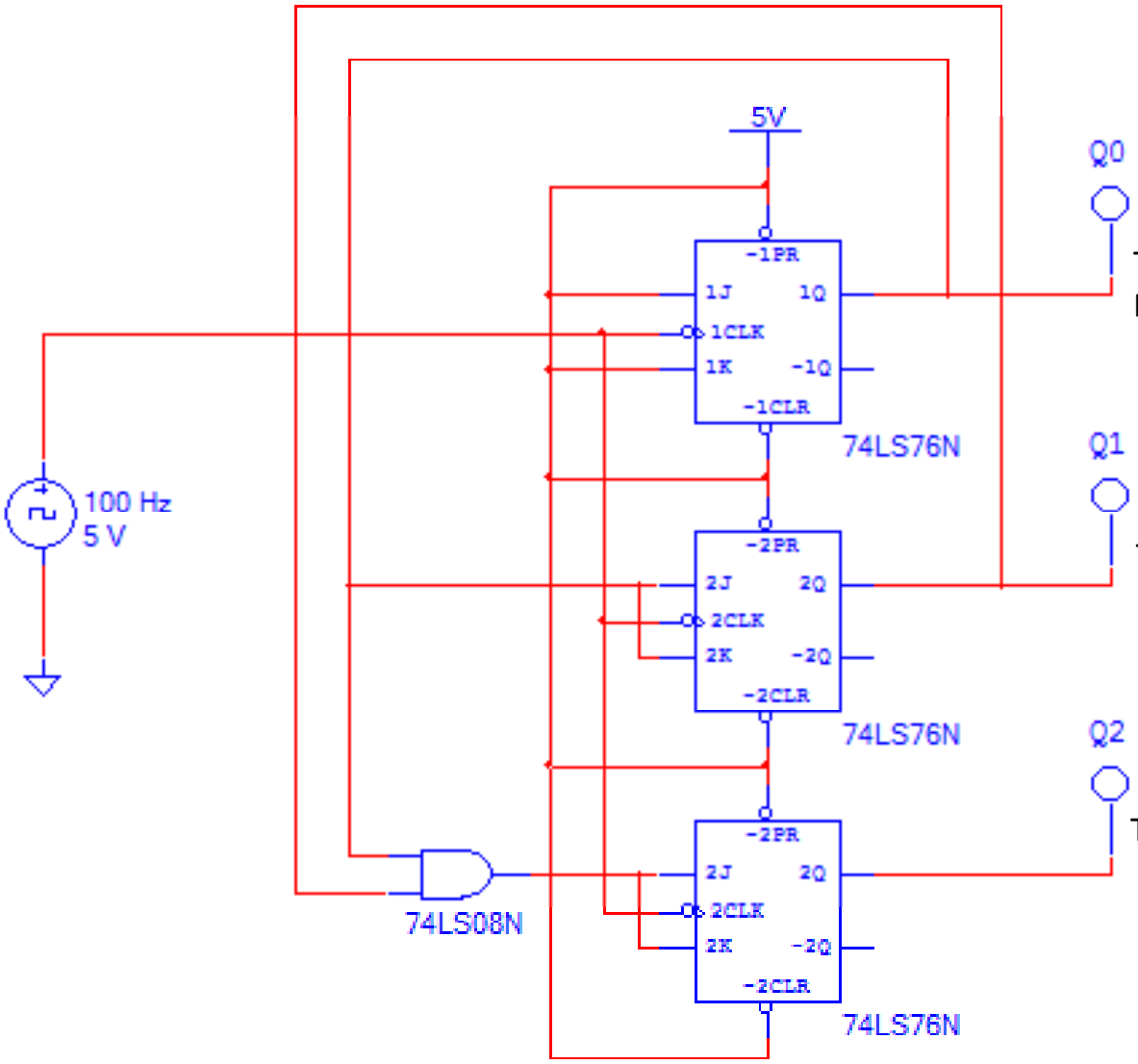




74LS47 Design Example



3-Bit Synch Up Counter: Circuit



Toggles On:
Falling Edge of CLOCK

Toggles On:
Falling Edge of CLOCK AND Q0=1

Toggles On:
Falling Edge of CLOCK AND Q0=1 & Q1=1

74LS193 Design Example #2